REMARKS

By this amendment claims 1, 7-10, and 15-16 have been amended, claims 3-6 and 11-14 have been cancelled without prejudice, and new claims 17-28 have been added. Accordingly, claims 1, 2, 7-10, and 15-28 are pending in the present application. The claim amendments and new claims are supported by the specification and claims as originally filed, with no new matter being added. Accordingly, favorable reconsideration of the pending claims is respectfully requested.

Applicants gratefully acknowledge the Examiner's indication that claims 7-8 and 15-16 are allowed, and that claims 4-5 and 12-13 would be allowable if rewritten in independent form. Claims 7, 8, 10, and 15-16 have been amended to delete unnecessary terminology and for clarity.

1. Objection to Claim 4

Claim 4 has been objected to for containing typographical errors. By this Amendment and Response, claim 4 has been cancelled and new claim 17 has been added to present former claim 4 in independent form. Accordingly, the objection to claim 4 is now moot.

2. Rejections Under 35 U.S.C. § 103(a)

Claims 1-3, 6, 9-11 and 14 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,780,908 to Sekiguchi et al. (hereinafter ("*Sekiguchi*") in view of U.S. Patent No. 6,077,774 to Hong et al. (hereinafter ("*Hong*") for the reasons set forth on pages 2-3 of the Office Action. Applicants respectfully traverse.

Claims 3, 6, 11, and 14 have been cancelled. Independent claim 1 has been rewritten to incorporate the limitations of claim 5, which the Examiner has indicated contains allowable

subject matter. Independent claim 9 has been rewritten to incorporate the limitations of claim 13, which the Examiner has indicated contains allowable subject matter. Claims 2 and 10 depend from claims 1 and 9, respectively, and thus include the limitations thereof. Accordingly, Applicants submit that claims 1-2 and 9-10 are in condition for allowance.

Claims 1-3, 6, 9-11 and 14 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over *Sekiguchi* in view of U.S. Patent No. 6,114,238 to Liao (hereinafter ("*Liao*") for the reasons set forth on pages 3-4 of the Office Action. Applicants respectfully traverse.

For the reasons stated above, Applicants submit that claims 1-2 and 9-10 are in condition for allowance.

Claims 1 and 9 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over *Liao* for the reasons set forth on pages 4-5 of the Office Action. Applicants respectfully traverse.

For the reasons stated above, Applicants submit that claims 1 and 9 are in condition for allowance.

Accordingly, Applicants respectfully request that the rejection of the claims under 35 U.S.C. § 103(a) be withdrawn.

3. New Claims

Claim 18 depends from claim 17, which was previously identified as former claim 4, rewritten in independent form. Claim 18 therefore contains the limitations of claim 17. Claim 19 includes the limitations of former claim 12, rewritten in independent form to include the limitations of claim 9, from which former claim 12 depended. Claim 20 depends from claim 19, and contains the limitations thereof. Accordingly, Applicants submit that claims 17-20 are in condition for allowance.

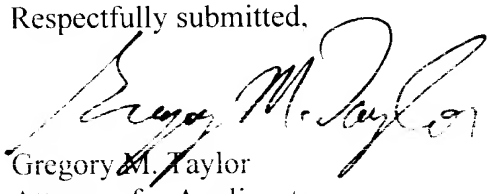
Claims 21-28 have been added to recite that the ammonia derivative comprises nitrogen-containing silane. Support for these claims can be found on page 12, lines 22-23 of the specification.

CONCLUSION

In view of the foregoing, Applicants respectfully request favorable reconsideration and allowance of the present claims. In the event the Examiner finds any remaining impediment to the prompt allowance of this application which could be clarified by a telephone interview, the Examiner is respectfully requested to contact the undersigned attorney.

Dated this 1st day of June 2001.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW THE CHANGES MADE

In the claims:

Claims 1 and 7-9 have been amended as follows:

1. (Once Amended) A semiconductor structure comprising:

an electrically conductive interconnect disposed within a first dielectric layer, said electrically conductive interconnect having an upper surface;

a [first] passivation layer disposed upon said upper surface, said [first] passivation layer comprising ammonia or derivatives thereof adsorbed upon said upper surface [including chemical reaction products and solid solution mixtures between said electrically conductive interconnect and a chemical compound]; and

an interlayer dielectric [ILD] disposed upon said first dielectric layer and upon said upper surface, said interlayer dielectric [ILD] being continuously adhered to said upper surface.

7. (Once Amended) A semiconductor structure comprising:

an electrically conductive interconnect having an upper surface and being disposed within a dielectric layer, said electrically conductive interconnect including:

a titanium liner layer disposed within a depression in said dielectric layer;

a titanium nitride layer disposed upon said titanium liner layer; and

a tungsten film disposed upon said titanium nitride layer and filling said depression;

a first passivation layer comprising a tungsten nitride compound and being disposed upon said upper surface;

a second passivation layer comprising ammonia or [and its] derivatives thereof [that is] adsorbed upon said first passivation layer; and

an interlayer dielectric [ILD] disposed upon said dielectric layer and upon said upper surface, said interlayer dielectric [ILD] being continuously adhered to said upper surface.

8. (Once Amended) A semiconductor structure comprising:

an electrically conductive interconnect disposed within a dielectric layer, said electrically conductive interconnect having an upper surface and including:

a titanium liner layer disposed within a depression in said dielectric layer;

a titanium nitride layer disposed upon said titanium liner layer; and

a tungsten film disposed upon said titanium nitride layer and filling said depression;

a passivation layer disposed upon said upper surface comprising ammonia or [and its] derivatives thereof [that is] adsorbed upon said upper surface; and

an interlayer dielectric [ILD] disposed upon said dielectric layer and upon said upper surface, said interlayer dielectric [ILD] being continuously adhered to said upper surface.

9. (Once Amended) An interconnect in an electronic device comprising:

a metallic first structure disposed within a first silicon oxide layer, said metallic first structure having an upper surface;

a [first] passivation layer disposed upon said upper surface, said [first] passivation layer comprising ammonia or derivatives thereof adsorbed upon said upper surface [including chemical reaction products and solid solution mixtures between said metallic first structure and a chemical compound]; and

a second silicon oxide layer disposed upon said first silicon oxide layer and upon said upper surface, said second silicon oxide layer being continuously adhered to said upper surface.

10. (Once Amended) An interconnect in an electronic device according to Claim 9, wherein said metallic first structure further comprises:

a [first] titanium liner layer disposed within an interconnect corridor in said first silicon oxide layer;

a [first] titanium nitride layer disposed upon said [first] titanium liner layer; and

a tungsten film disposed upon said [first] titanium nitride layer.

15. (Once Amended) An interconnect in an electronic device comprising:

a metallic structure disposed within a first silicon oxide layer, said metallic structure having an upper surface and including:

a titanium liner layer disposed within an interconnect corridor in said first silicon oxide layer;

a titanium nitride layer disposed upon said titanium liner layer; and

a tungsten film disposed upon said titanium nitride layer;

a first passivation layer disposed upon said upper surface and [composed] comprised of a tungsten nitride compound;

a second layer comprising ammonia or [and its] derivatives thereof [that is] adsorbed upon said first passivation layer; and

a second silicon oxide layer disposed upon said first silicon oxide layer and upon said upper surface, said second silicon oxide layer being continuously adhered to said upper surface.

16. (Once Amended) An interconnect in an electronic device comprising:

a metallic structure disposed within a first silicon oxide layer, said metallic structure having an upper surface and including[;]:

a titanium liner layer disposed within an interconnect corridor in said first silicon oxide layer;

a titanium nitride layer disposed upon said titanium liner layer; and

a tungsten film disposed upon said titanium nitride layer;

a passivation layer disposed upon said upper surface and comprised [composed] of ammonia or [and its] derivatives thereof [that is] adsorbed upon said upper surface; and

a second silicon oxide layer disposed upon said first silicon oxide layer and upon said upper surface, said second silicon oxide layer being continuously adhered to said upper surface.